

U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	A	R	...
1		US 20020034620	20020305	31	Integrated circuit memory devices having non-volatile	4387101			Yoshida, Kenji et al.	Y	Y	Y	Y	Y	Y
2		US 20020036965	20020307	21	METHODS OF FORMING PROCESSSED SEMICONDUCTOR GRAIN FILLS	4387102			Yoshida, Kenji et al.	Y	Y	Y	Y	Y	Y
3		US 20020036541	20020307	191	Twisted Arrays And Charge Storage Devices, And Methods	4387103			Yoshida, Kenji et al.	Y	Y	Y	Y	Y	Y
4		US 20020027227	20020307	21	SEMICONDUCTOR MEMORY DEVICE HAVING A TRENCH AND A GATE	4387104			KAWA, SEEN-SUN	Y	Y	Y	Y	Y	Y
5		US 20020025479	20020308	96	Process for fabricating semiconductor integrated	4387105	3587130 4387106		Okamoto, Yoshihiro et al.	Y	Y	Y	Y	Y	Y
6		US 20020037901	20020314	94	Electrically programmable memory element with raised	4387106			Killey, Patrick et al.	Y	Y	Y	Y	Y	Y
7		US 20020017069	20020214	121	Semiconductor integrated circuit device, process for	4387107	4387108 4387109		Yoshida, Kenji et al.	Y	Y	Y	Y	Y	Y
8		US 20020016734	20020217	74	Manufacturing method of semiconductor integrated	4387108	4387109 4387110		Yoshida, Kenji et al.	Y	Y	Y	Y	Y	Y
9		US 20020016661	20020217	101	Manufacturing method of photomask and photomask	4387109	4387110 4387111		Kawaguchi, Naoki et al.	Y	Y	Y	Y	Y	Y
10		US 20010075543	20020117	69	Manufacturing method of semiconductor integrated	4387110	4387111		Hayashi, Kazuo et al.	Y	Y	Y	Y	Y	Y
11		US 20020016669	20020220	25	Method of fabricating display device	4387111	4387112 4387113		Nagao, Futoshi et al.	Y	Y	Y	Y	Y	Y

1/1 PLUSPAT - (C) QUESTEL-ORBIT

PN - US5710461 A 19980120 [US5710461]

TI - (A) SRAM cell fabrication with interlevel dielectric planarization

PA - (A) SGS THOMSON MICROELECTRONICS (US)

IN - (A) NGUYEN LOI (US); SUNDARESAN RAVISHANKAR (US)

AP - US78142997 19970110 [1997US-0781429]

PR - US16933893 19931217 [1993US-0169338]

- US32873695 19951025 [1995US-0328736]

- US78142997 19970110 [1997US-0781429]

IC - (A) H01L-023/48 H01L-023/522 H01L-029/34 H01L-029/54

EC - H01L-021/3105B

- H01L-021/8244

PCL - ORIGINAL (O) : 257754000; CROSS-REFERENCE (X) : 257350000 257380000
257381000 257385000 257640000 257740000 257752000 257758000
257903000 257904000

DT - Basic

CT - US4676867; US4797717; US4920071; US4975875; US4990998; US5001539;

US5077238; US5083190; US5110763; US5132774; US5151376; US5159416;

US5169491; US5177238; US5188987; US5204288; US5219792; US5290399;

US5319247; US5373170; US5381046; US5534731; US5552628; JP0099243;

JP0135044; JP2251722; WO8700828

- IEEE Electron Device Letters, vol. 12, No. 3, Mar. 1991, Hot-Carrier
Aging of the MOS Transistor in the Presence of Spin-On Glass as the
interlevel Dielectric, by N. Lifshitz and G. Smolinsky, pp. 140-142.

Journal Electrochem. Soc., vol. 139, No. 2, Feb. 1992, Three "Lot Dt"
Options for Planarizing the Pre-Metal Dielectric on an Advanced Double
Poly BiCMOS Process, by W. Dauksner, M Miller, and C. Tracy, pp.
532-536.

Journal Electrochem. Soc., vol. 139, No. 2, Feb. 1992, Polysilicon
Planarization Using Spin-On Glass, by Shrinath Ramaswami and Andrew
Nagy, pp. 591-599.

Journal Electronicem. Soc., vol. 140, No. 4, Apr. 1993, The Effect of
Plasma Cure Temperature on Spin-On Glass, by Hideo Namatsu and
Kazushige Minegishi, pp. 1121-1125.

STG - (A) United States patent

AB - A 4-T SRAM cell in which two layers of permanent SOG (with an
intermediate oxide layer) are used to provide planarization between
the first and topmost poly layers.

1/1 LGST - (C) LEGSTAT

PN - US 5710461 [US5710461]

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DT - US-P

ACT - 19970110 US/AE-A

APPLICATION DATA (PATENT)

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- 19980120 US/A

PATENT

- 20000307 US/RF

REISSUE APPLICATION FILED

20000120

UP - 2000-10

1/1 CRXX - (C) CLAIMS/RRX

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PT - E (Electrical)

PA - SGS-Thomson Microelectronics Inc

ACT - 20000120 REISSUE REQUESTED

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UP - 2000-10

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1/1 PAST - (C) PAST

AN - 200010-001243

PN - 5710461 A [US5710461]

DT - A (UTILITY)

OG - 2000-03-07

CO - REA

ACT - REISSUE APPLICATION FILED

SH - REISSUE APPLICATION FILED

1/39/4

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Basic Patent (No,Kind,Date): US 5395785 A 19950307 <No. of Patents: 002>

Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date
US 5395785	A	19950307	US 169338	A	19931217 (BASIC)
US 5710461	A	19980120	US 781429	A	19970110

Priority Data (No,Kind,Date):

US 169338 A 19931217
US 781429 A 19970110
US 328736 B1 19951025
US 169338 A3 19931217

PATENT FAMILY:

UNITED STATES OF AMERICA (US)

Patent (No,Kind,Date): US 5395785 A 19950307

SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION
(English)

Patent Assignee: SGS THOMSON MICROELECTRONICS (US)

Author (Inventor): NGUYEN LOI (US); SUNDARESAN RAVISHANKAR (US)

Priority (No,Kind,Date): US 169338 A 19931217

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National Class: * 437052000; 437047000; 437060000; 437235000;
437919000

IPC: * H01L-021/70

CA Abstract No: * 122(24)304566E; 122(24)304566E

Derwent WPI Acc No: * C 95-114834; C 98-238649; C 95-114834

Language of Document: English

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19951025; US 169338 A3 19931217

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257758000

IPC: * H01L-029/34; H01L-023/48; H01L-023/522; H01L-029/54

CA Abstract No: * 122(24)304566E

Derwent WPI Acc No: * C 95-114834; C 98-238649; C 98-238649

Language of Document: English

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US 5395785 P 19931217 US AE APPLICATION DATA (PATENT)
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US 5395785 P 19931217 US AS02 ASSIGNMENT OF ASSIGNOR'S
INTEREST

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NGUYEN, LOI N. : 19931217; SUNDARESAN,
RAVISHANKAR : 19931217

US 5395785	P	19950307	US A	PATENT
US 5710461	P	19931217	US AA	PRIORITY
		US 169338	A3	19931217
US 5710461	P	19951025	US AA	PRIORITY
		US 328736	B1	19951025
US 5710461	P	19970110	US AE	APPLICATION DATA (PATENT)
				(APPL. DATA (PATENT))
		US 781429	A	19970110
US 5710461	P	19980120	US A	PATENT
US 5710461	P	20000307	US RF	REISSUE APPLICATION FILED
				(REISSUE APPL. FILED)
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